IC 製程簡介

FAB4 DRAM Process Integration

Contents

Thermal oxidation (熱氧化) :

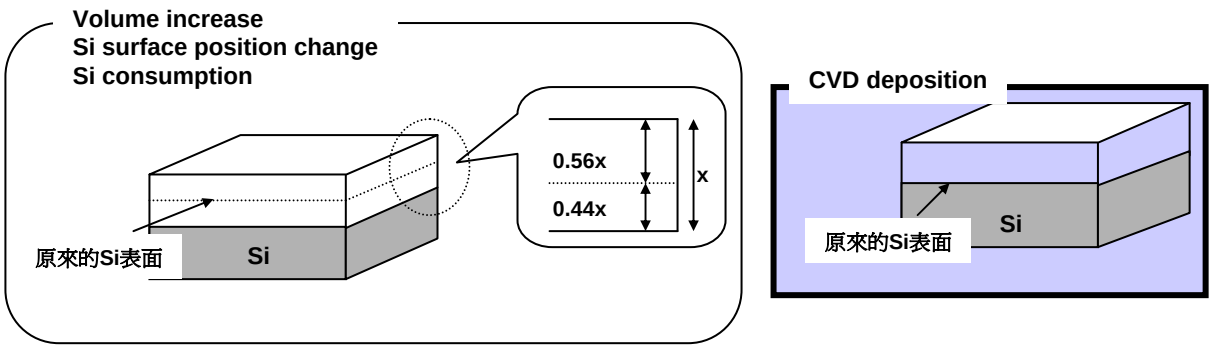
[1] 原理 – 在高溫氧化爐**(oxidation furnace)**中利用高純度的**O_2**或水蒸氣將**Si** 反應成**SiO_2**

[2] 方式 – 乾式**(dry)**氧化 **$Si + O_2 \rightarrow SiO_2$**
-- 濕式**(wet)**氧化 **$Si + 2H_2O \rightarrow SiO_2 + 2H_2$**

[3] 機台 – 水平式 → **5“ wafer** 以下使用
-- 垂直式 → **6“ wafer** 以上使用**(**節省機台所佔面積**)**

[4] 特性 –

a. 成長特性



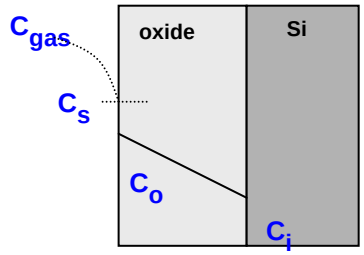
氧化速率(Rox)

- oxidant species : ↑ Rox ↑
- temperature : ↑ Rox ↑
- substrate doping : B enhanced
- wet type > dry type

⇔

熱氧化模 型 (Deal-Grove Model)

- 反應氣體須到達gas-oxide界面
- 反應氣體須穿過(擴散)已存在的 oxide layer
- 反應氣體在Si表面起反應



b. 氧化層特性

依成長方式

生長方式	Density	蝕刻率(HF solution)
dry	high	Low
wet	↓	↓
CVD		
PECVD	low	high

依成長溫度

生長溫度	Density
low(600C)	high
↓	↓
high(1150C)	low

評估氧化層

- 厚度 (thickness)
- 屈折律率(refractive index)
- 蝕刻率(etching rate)
- 氧化層中電荷(charge)
- oxide/Si 界面(interface)
- 氧化層介電破壞(breakdown)

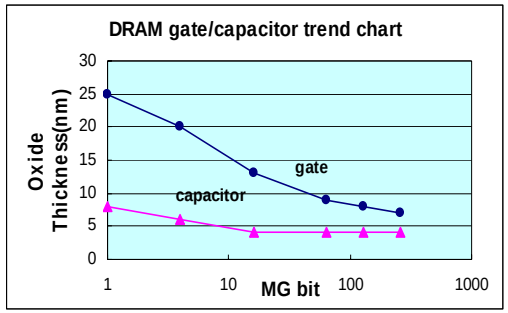
[5] 應用：

thickness	application
30~100A	*gate oxide*, tunneling
150~500A	capacitor dielectrics
200~500A	LOCOS pad-oxide
2000~5000A	field oxide

防止Na 污染：
Na離子 --> 電晶體電性變差
1. 氧化時添加 HCl (3~5%)
2. PSG getter layer
3. Si_3N_4 diffusion barrier

[6] 未來趨勢 --

1. very thin, defect-free oxide film
2. 大尺寸化熱處理條件



Doping (摻雜)：將不純物(dopant), 如 B, P 加入Si中, 藉此改變Si type及電性

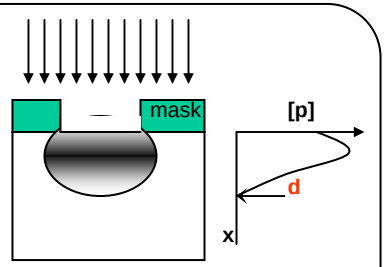
[1] 方式 – 離子植入(ion implantation)法
-- 擴散(diffusion)法

[2] 機台 – ion implantation → implanter
-- diffusion → furnace

[3] 原理 –

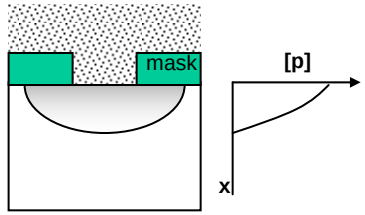
Ion implantation

- 將dopant離子化後, 利用電場加速之, 使其具備所需的能量後, 將離子射進Si中
- 一般分成blanket或masked implantation



Diffusion

- 將氣體化的dopant, 藉擴散的自然現象, 由Si表面進入Si中. 或將固態的dopant source成長於Si surface, 藉高溫擴散進入Si內
- 一般亦分成blanket或masked implantation



差異點

- doping profile -
  擴散法 - 表面濃度最高
  植入法 - 因植入能量而定
- lateral(側向) diffusion -
  擴散法 > 植入法

植入法的優勢

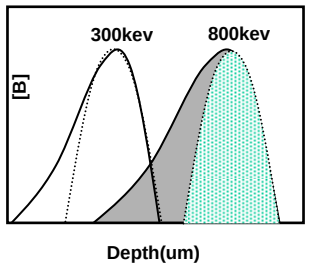
- doping profile 的控制 - easy
- little lateral diffusion - dimension shrinkage

[4] 植入法的特性(缺點) --

Atom back-scattering

- dopant離子射入Si時, 除了會沿入射方向前進外,亦有部份離子會被反向散射
- 一般而言, 質量越輕的離子此現象越明顯

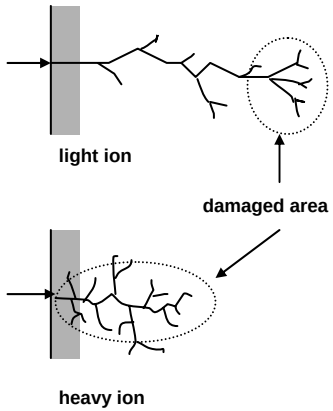
==>>
非預期的doping profile



Damage

- dopant離子射入Si時, 是靠與矽原子的碰撞喪失能量後才停在預期的深度, 而矽原子也因此可能被撞離原來所在的晶格位置, 此稱之

==>>
leakage path

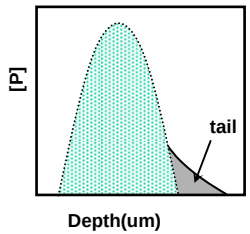


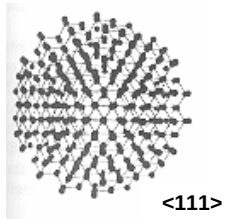
- 解決方法:
  熱處理, 在N2 or Ar 環境中加高溫使矽原子回到正常的晶格位置(回火處理)

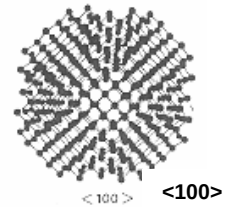
Channeling effect

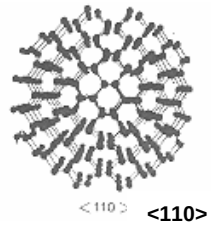
- dopant離子進入Si內, 因Si 爲單晶結構, 朝某個方向看去時其空間相對鬆散, 離子穿入較深的深度

==>
非預期的doping profile







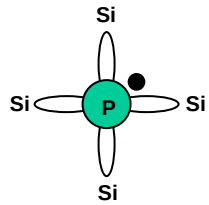


•解決方法:
1. Wafer tilt angle 7 deg.
2. Amorphous buffer layer

活化(activation)

- dopant離子射入Si後, 是在interstitial site, 必須位於substitutional site(即正常的晶格位置), 與矽原子鍵結後, 才會改變所摻雜區域的type

- 通常使用RTP來完成

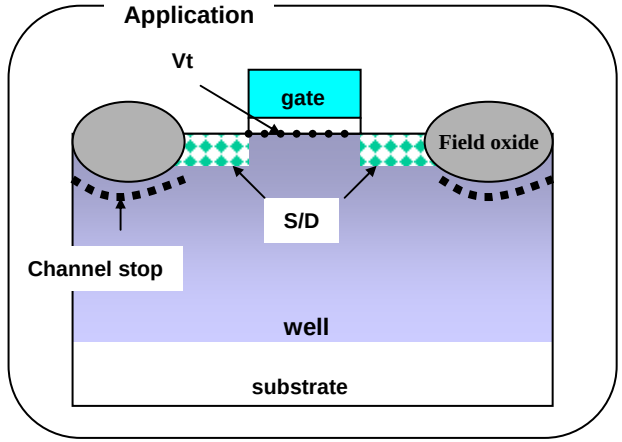


N-type

[5] Implanter的種類 /應用--

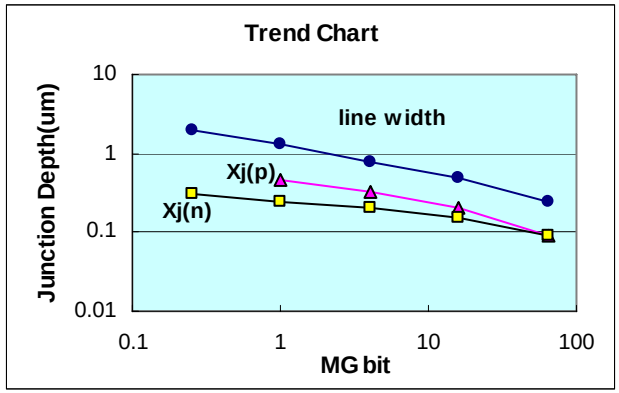
1. **Medium current implanter <--精確控制dose 量**
   well/ Vt / channel stop 植入
2. **High current implanter <-- high dose 量需求**
   汲極/源極 植入, poly load
3. **High energy implanter <-- 深度需求**
   retrograde well, buried layer

➔ **MOS電性調整**



[6] 未來趨勢--

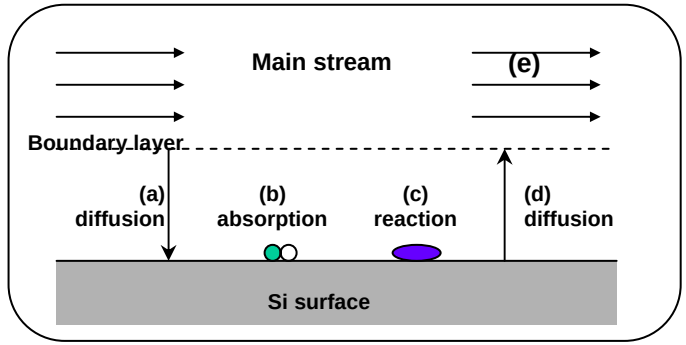
1. **淺接面(shallow junction)**
   --> low junction capacitance
   --> small later diffusion
2. **Little charge damage/high throughput 機台**
3. **短時間回火技術開發**
   --> for shallow junction



CVD (chemical vapor deposition) : 化學氣相沉積

[1] 原理 – 氣相反應物在**Si surface**發生化學反應, 成長出所需之薄膜

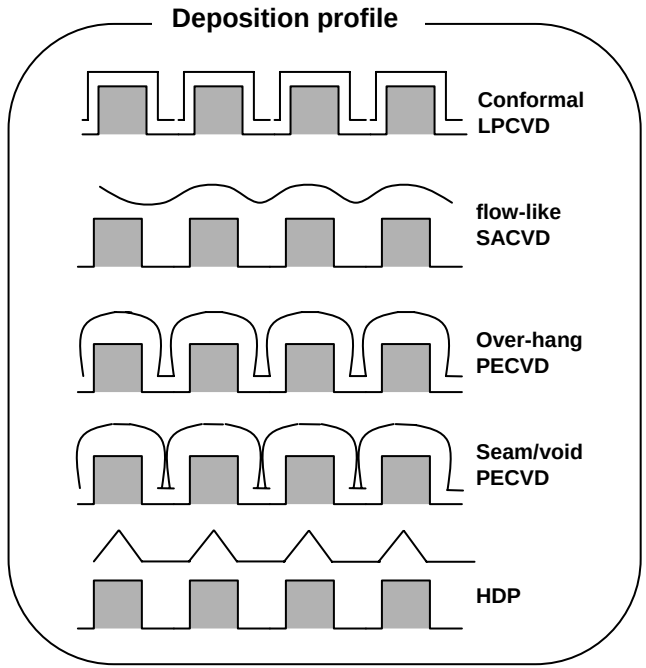
(* 若化學反應未到達Si surface即發生, 此即爲particle)



[2] 方式 –

依反應室**(chamber)**的氣壓及電磁環境可分成:

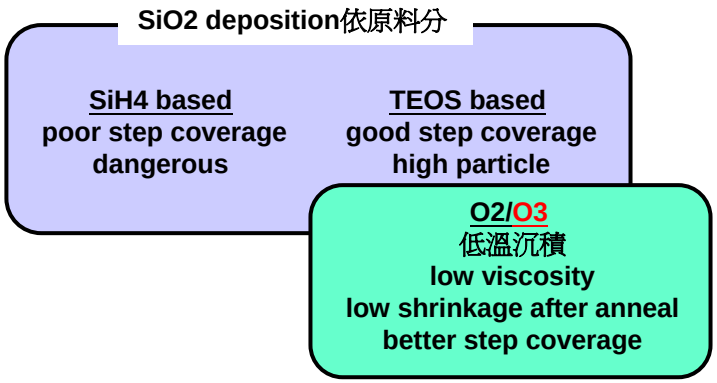
1. **APCVD (atmospheric pressure) CVD**
   - **-- high deposition rate/ throughput**
2. **SACVD (sub-atmospheric) CVD:50~600torr**
   - **-- flow-like deposition**
3. **LPCVD (low pressure) CVD: 0.1~10torr**
   - **-- good uniformity/ conformal**
4. ***PECVD**** **(plasma enhanced) CVD: 0.1~10torr**
   - **-- low temperature**
5. ***HDPCVD**** **(high density plasma) CVD:**
   - **-- good gap fill**



***** 在有**plasma(電漿)**的環境下完成, 須注意
– charge damage, film的純度

[3] 薄膜種類 --

material	反應氣體	Method	溫度©	用途	Remark
poly-Si	SiH4	LP	500~700	半導体	溫度控制結晶度
Si3N4	DCS+NH3	LP	750~850	barrier	reduce H含量
	SiH4+NH3+N2	PE	350~400	passivation	
SiO2	SiH4+O2(PH3+B2H6)	AP	400~480		doped
	SiH4+O2(PH3+BCl3)	LP	650~750		doped
	SiH4+N2O(PH3+B2H6)	PE	200~400		doped
	DCS+N2O	LP	750~850		reduce H含量
	TEOS(PH3, TMP)	LP	650~750	isolation	doped(TEOS)
	TEOS+O2(PH3, TMP)	PE	350~500		doped(TEOS)
	TEOS+O3	AP, LP	350~500		
	TEOS+O3(TMP, TMB)	AP	350~500		doped(BPSG)
WSi	WF6+SiH4	LP	300~400	導線	
Cu	Cu^{I}(hfac)(tmvs), Cu^{II}(hfac)2+H2	LP	350~450	導線	
W	WF6+H2	LP	400~500	導線	
	WF6+SiH4	LP	"		
TiN	TiCl4+NH3	LP	400~700	barrier	
	TDEAT+NH3	LP	"	ARC	
	TDMAT(+NH3)	LP	"		
Al	DMAH Dimer Thermal decomposition	LP	150~300	導線	



[4] 影響沉積的參數 --

1. Pressure
2. Temperature
3. Reactant concentration
4. dopants

PVD (physical vapor deposition) : 物理氣相沉積

[1] 原理 – 氣相反應物沉積在**Si surface**以成長出所需之薄膜
(並未發生化學反應)

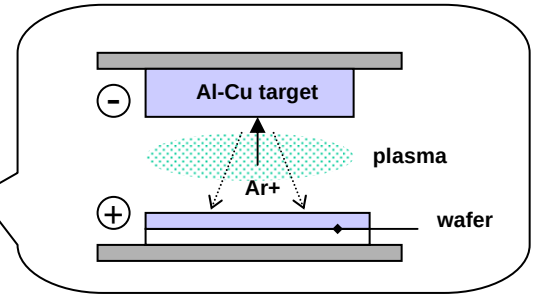
[2] 方式 –

1. Sputtering(濺鍍)

-- 利用**Ar**離子對靶材(target)進行轟擊(bombardment), 轟出靶材表面的原子或原子團,而後吸附在晶片上以生成薄膜

2. Evaporation(蒸鍍)

-- 利用電子束或電阻加熱薄膜材使其氣化而被晶片表面吸附以形成薄膜



[3] 應用 –

1. Al-Si-Cu :

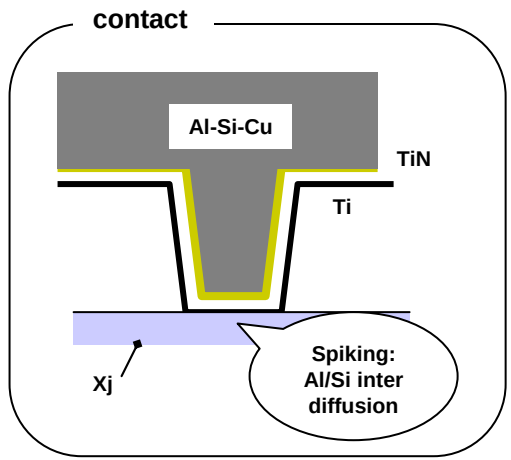
Al- low resistance, good interface property between dielectrics

Si- 避免spiking

Cu-增加 金屬線抗EM(electron migration)

2. Ti : 降低**contact**阻值, 除去**native oxide**

3. TiN : 擴散障層



[4] CVD/PVD 比較 –

1. 製程複雜度：

CVD > PVD--> why need CVD?

2. 填洞(gap fill)能力：

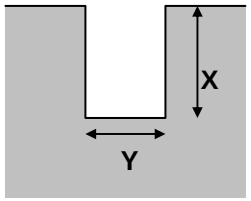
CVD > PVD

****** 比較**gap fill**能力的兩個重要**factor：**

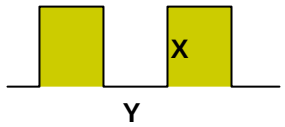
Aspect Ratio

Ratio： X/Y

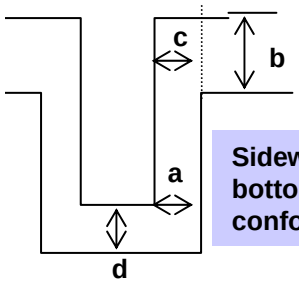
Contact/via case



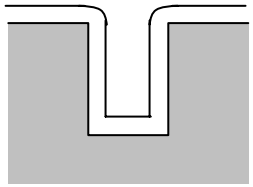
Line space case



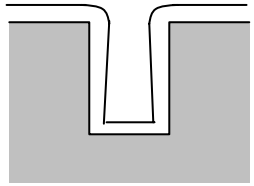
Step Coverage



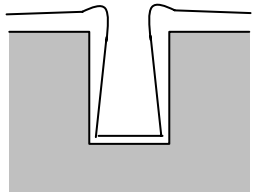
Sidewall step coverage = a/b
bottom step coverage = d/b
conformal = a/c



Uniform coverage from rapid surface migration



nonconformal coverage from little surface migration and long mean free path



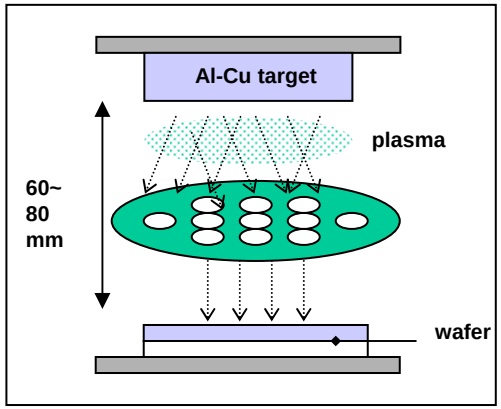
nonconformal coverage from no surface migration and short mean free path

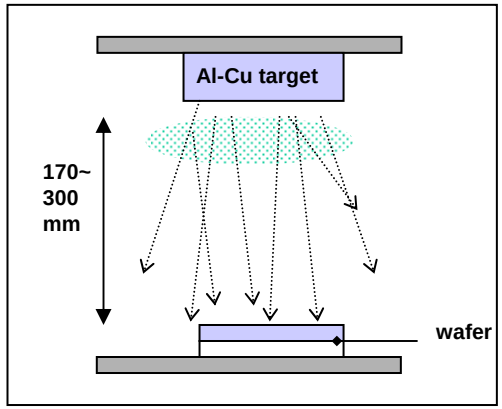
[5] 未來趨勢 –

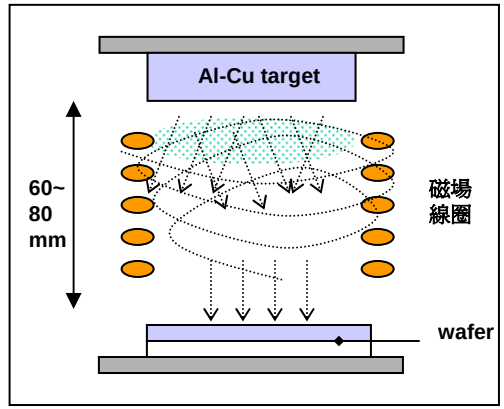
1. 改善 PVD 填洞能力：

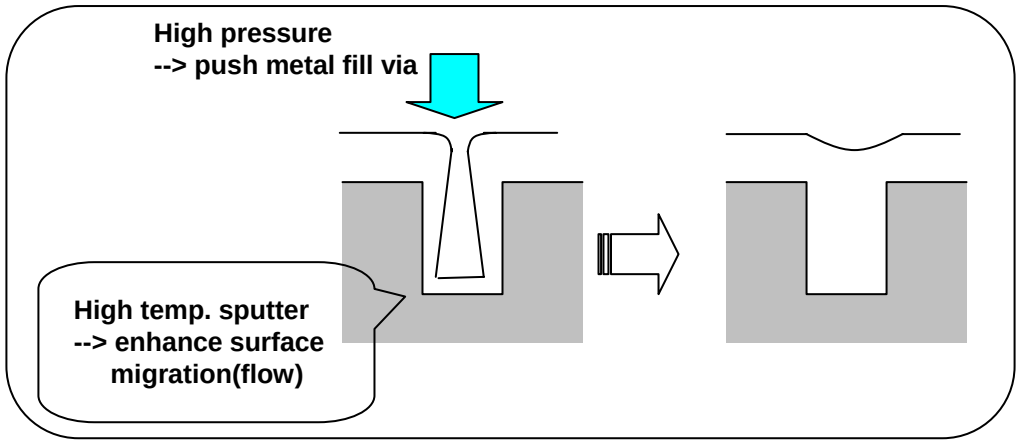
collimated sputter
LTS(long through sputter)
IMP(ion metallization plasma)
hot process/ high pressure process

2. CVD取代PVD

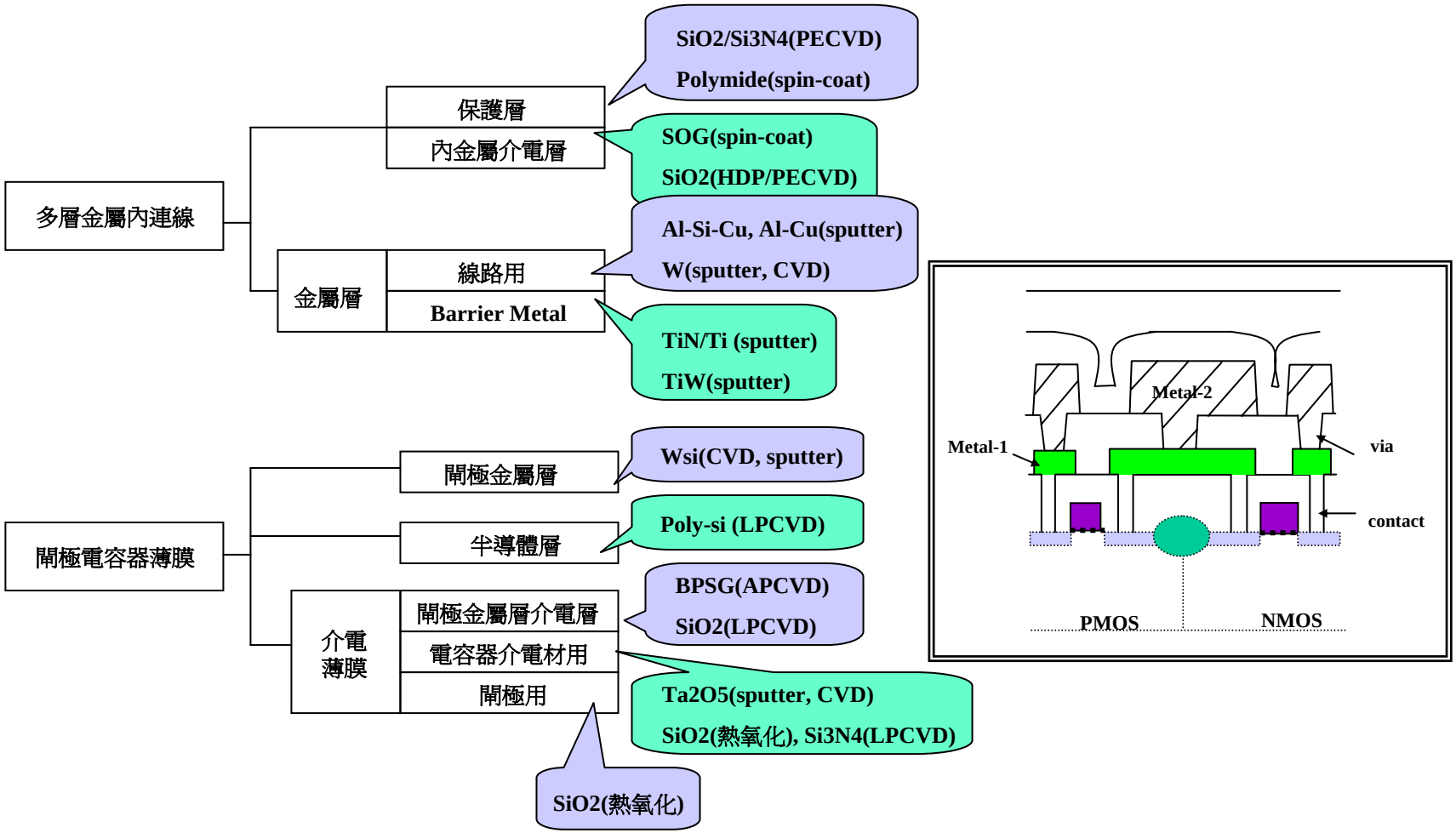








[6] 薄膜應用 –


多層金屬內連線
保護層
內金屬介電層
金屬層
線路用
Barrier Metal
SiO2/Si3N4(PECVD)
Polymide(spin-coat)
SOG(spin-coat)
SiO2(HDP/PECVD)
Al-Si-Cu, Al-Cu(sputter)
W(sputter, CVD)
TiN/Ti (sputter)
TiW(sputter)
閘極電容器薄膜
閘極金屬層
半導體層
介電
薄膜
閘極金屬層介電層
電容器介電材用
閘極用
Wsi(CVD, sputter)
Poly-si (LPCVD)
BPSG(APCVD)
SiO2(LPCVD)
Ta2O5(sputter, CVD)
SiO2(熱氧化), Si3N4(LPCVD)
SiO2(熱氧化)
Metal-2
Metal-1
via
contact
PMOS
NMOS

Photolithography (微影或黃光)：製作圖案(pattern)的方法

[1] 原理 – 將一層感光材料(光阻)均勻塗在晶片上, 使部份曝光部份未曝光後經過顯影, 則所需pattern留在晶片上

[2] 方式 --

1. 依光阻(resist)種類分：

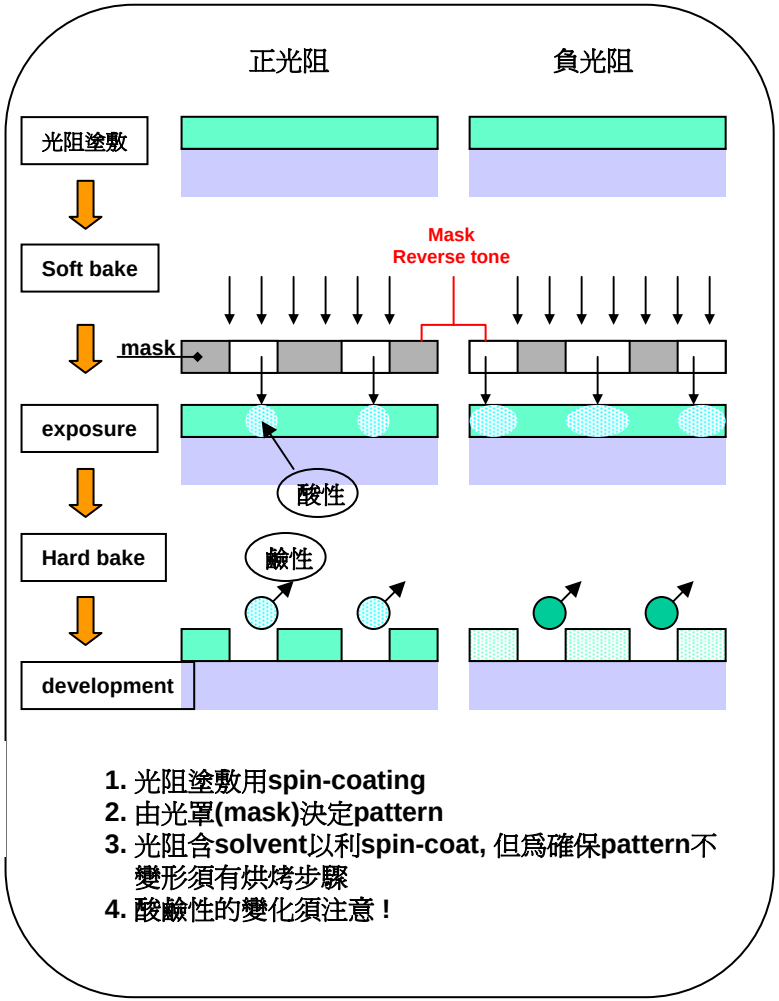
正光阻 -->(見光死)光阻本身不溶於顯影液, 曝光部份起化學反應在顯影過程時被溶於顯影液中

負光阻 -->光阻本身會溶於顯影液, 曝光部份起化學反應, 在顯影過程中不被溶解

** 負光阻解析度較差

2. 依曝光光源波長分：

g-line : 436 nm
I-line : 365 nm
DUV(deep UV) : 248nr (need new type resist -- chemical amplified resist)



1. 光阻塗敷用spin-coating
2. 由光罩(mask)決定pattern
3. 光阻含solvent以利spin-coat, 但爲確保pattern不變形須有烘烤步驟
4. 酸鹼性的變化須注意！

Why need DUV

Resolution limit, R = K1 * L/NA

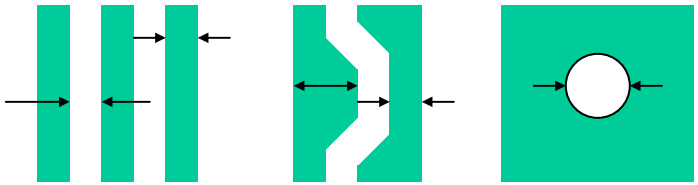
Depth of focus, DOF = K2 * L/NA^2

K1, K2 : constant related resist
L: wave length
NA : numerical aperture

[3] 應用時的重要評估項目 –

1. CD(critical dimension) :

通常量測 **pattern**中最小尺寸或特定之處, 以確保 **pattern**達到製程需求



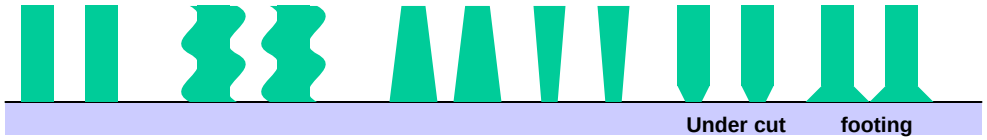
CD不合的原因有：

a. 製程參數不對 -- 多爲設定問題, 如曝光量, 景深用錯

b. 製程限制 -- 景深不足
-- 解析度不足
-- 光學效應(Proximity effect)

==> 解決方法: 從光源 --> Off-Axis illumination
從光罩 --> phase-shift mask
從layout --> OPC

2. Resist profile :



OK	Standing wave effect	DOF error	Development error (DUV resist case)
	Bottom ARC		

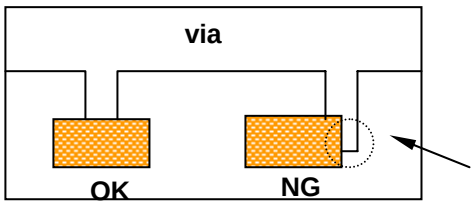
黃光的應用：

a. 離子植入時的mask

b. 蝕刻時的mask

3. Overlay : 前/後兩層微影對準度的check

有X & Y兩個方向



電性上 : Rc 偏高, 可靠度變差
製程上 : metal 填入不易

Etching(蝕刻)：

[1] 原理 – 利用化學反應有時加入物理性的撞擊, 將不需要材料除去

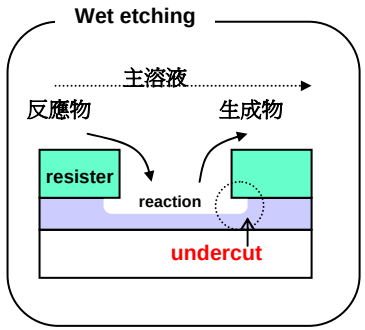
[2] 方式 --

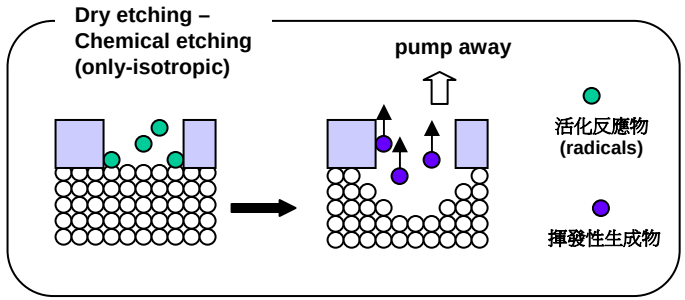
1. 溼式(wet)蝕刻：

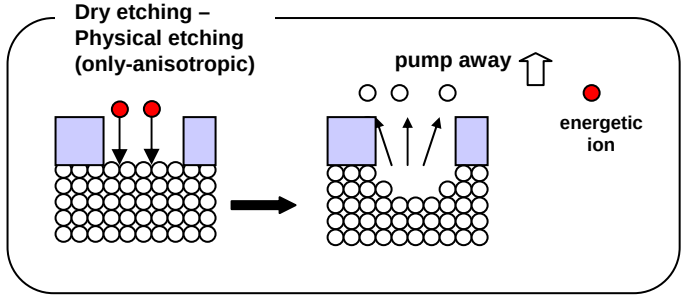
運用化學溶液進行蝕刻, 特徵爲只有化學反應, 爲等向性(isotropic)蝕刻

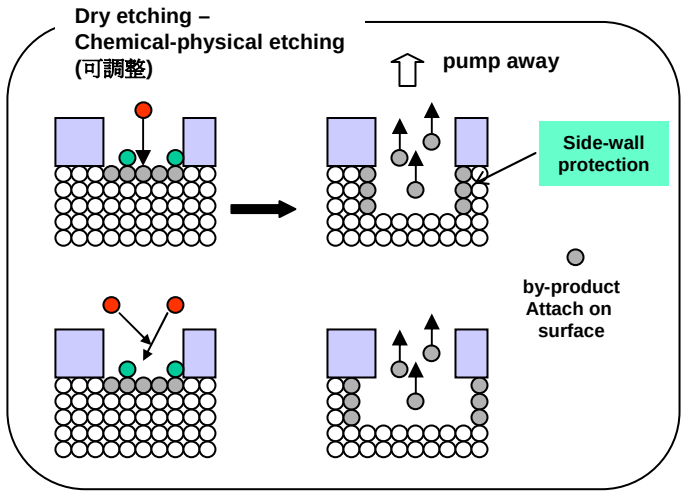
2. 乾式(dry)蝕刻：

運用電漿將蝕刻氣體離子化後, 與材料進行化學反應或加入物理性的撞擊, 具有等向或非等性(anisotropic)的特徵



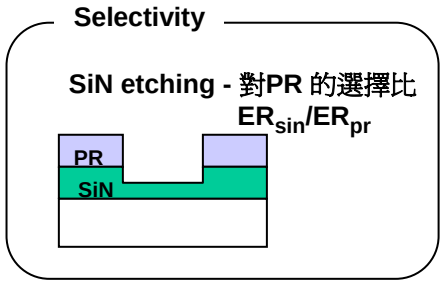


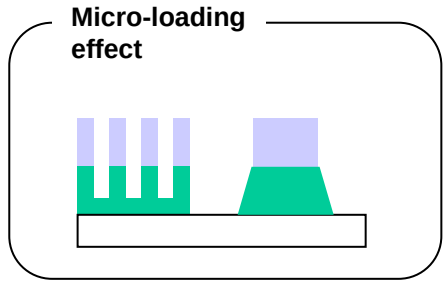


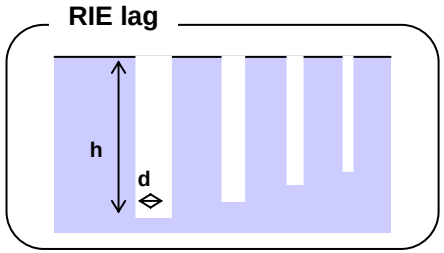


[3] 評估項目 –

1. 蝕刻率(ER)
2. 均勻性: U(%)=(max-min)/(max+min)
3. 選擇比(selectivity) = ER_1/ER_2
4. Etching bias=AEI-ADI
5. Profile
6. Micro-loading effect : 對不同的pattern density有不同ER & profile
7. Aspect ratio(AR) = h/d
8. RIE lag: ER reduce when AR increase







[4] 應用 –

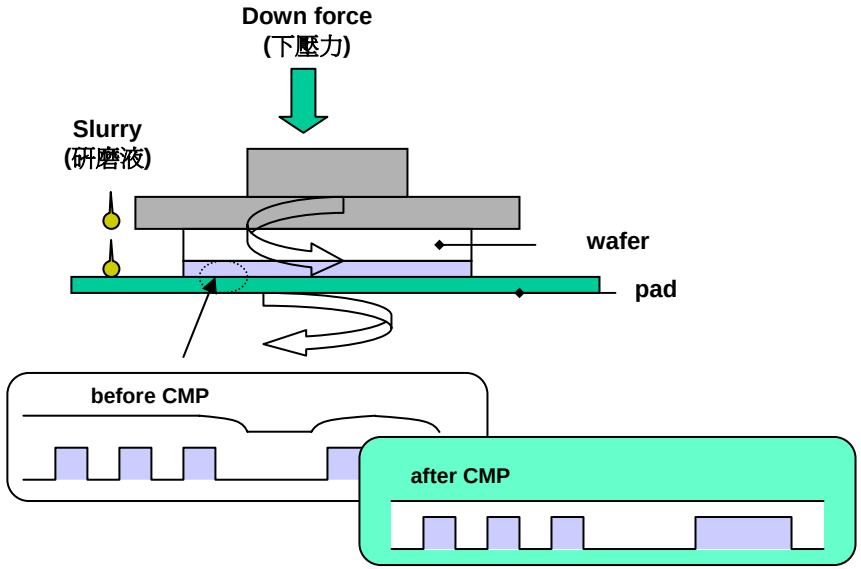
material	wet etching	dry etching
Si	HF + HNO3	(1) CF4 (2) CCl4 (3) SF6 (4) SF6 + C2ClF5
Si3N4	Hot H3PO4	(1) CF4
SiO2	HF	(1) C2F6, CHF3 (2) CF4 + H2
W	H3PO4 + HNO3	(1) CF4 + O2 (2) SF6
Al	H3PO4 + HNO3 + CH3COOH + H2O	(1) CCl4 (2) BCl3 + Cl2 (3) SiCl4

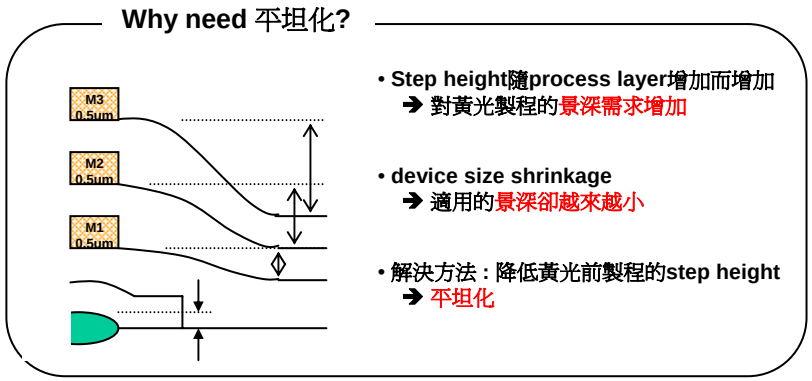
wet etching vs. dry etching

	Wet	Dry
Selectivity	excellent	Sometimes good/NG
Damage	no	need to be concerned (antenna effect)
Equipment	simple	complex
CD control	difficult	good
profile	isotropic	controllable

CMP(Chemical-Mechanical Polishing) :

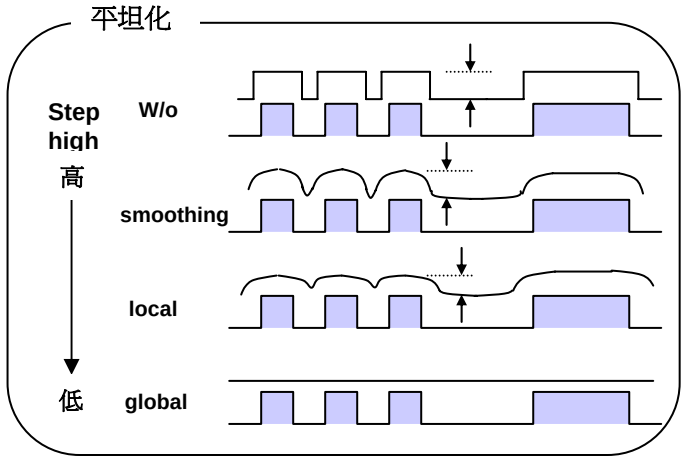
[1] 原理 – 如下圖所示



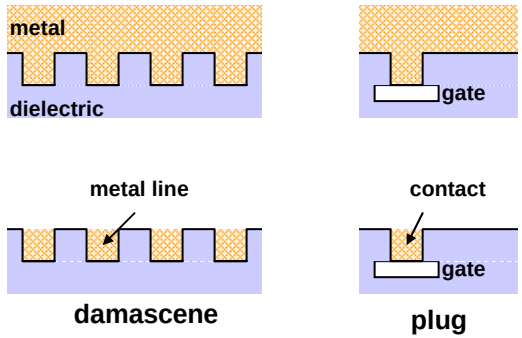


[2] 應用 --

1. 全面性(global)平坦化 : oxide CMP

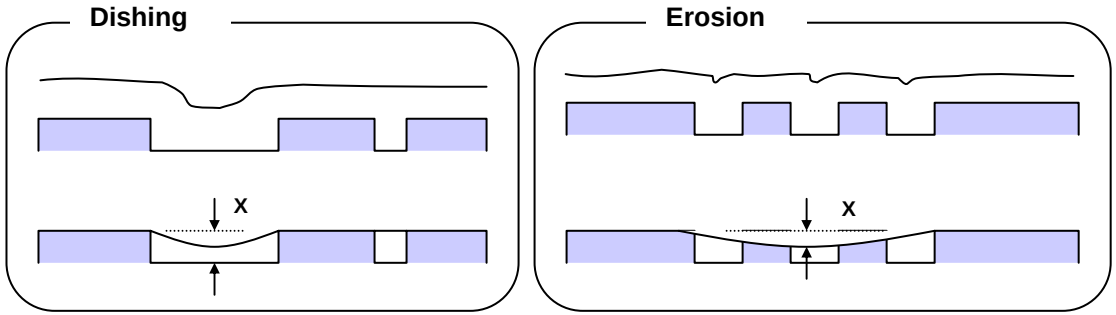


2. Strip material : W CMP



[3] 重要評估項目 –

1. 研磨速率(polishing rate)
2. 均勻度(uniformity)
3. 選擇比
4. Dishing
5. erosion
6. Scratch
7. Post-clean



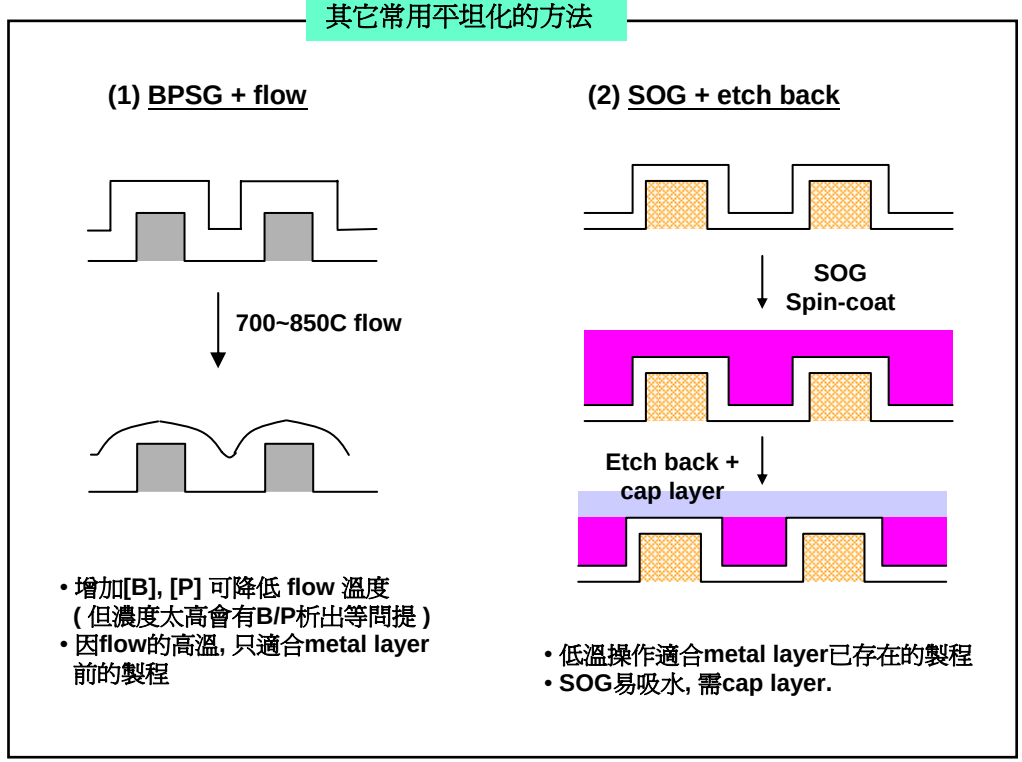
[4] Slurry的成份 –

1. 研磨劑(abrasive) :
   一般是氧化物, 如 Al_2O_3, CeO_2
2. 化學物質(chemicals) :
   一般爲氧化被研磨物表面用, 如 $Fe(NO_3)$, $K(IO_4)$, H_2O_2
3. Surfactant, suspension …
   控制slurry的酸鹼度 …

[5] 未來發展 –

1. Dishless CMP
2. Cu CMP
3. Al CMP

其它常用平坦化的方法

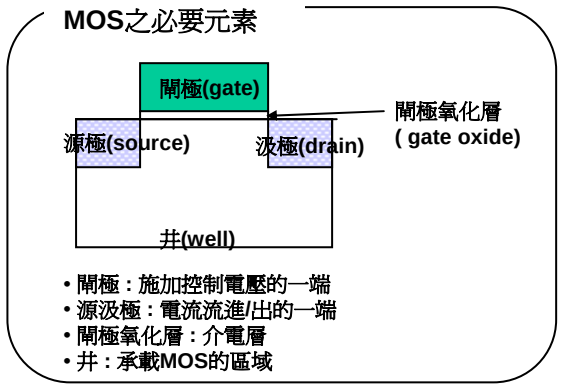


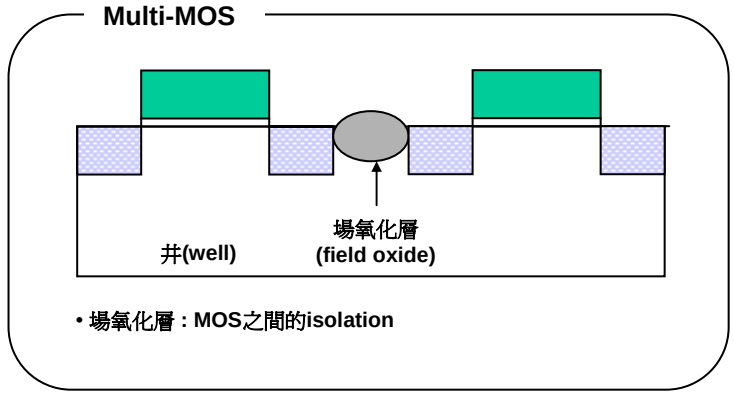
何謂MOS(Metal-Oxide-Semiconductor) :

[1] 定義 –

從製程上來說：指在半導體上製做出氧化層及金屬層等, 最後做出積體電路(ICs)的一種製程技術

從電路上來說：是指元件(device), 其功能爲“開關(switch)” 或是“電晶體(transistor)”

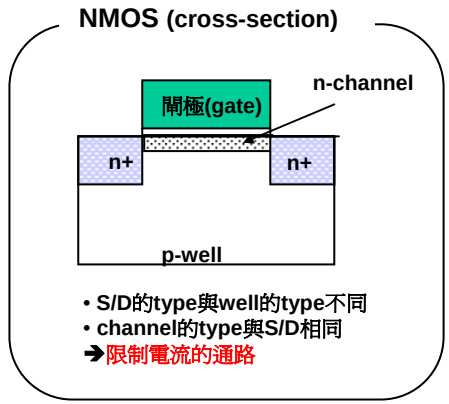


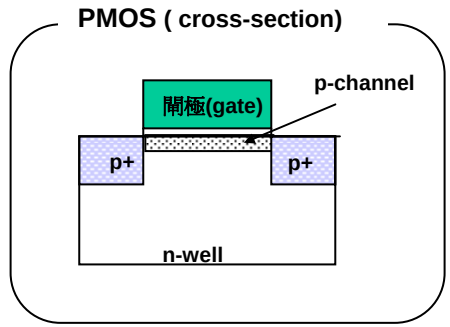


[2] 種類 –

1. NMOS : n-channel MOS
2. PMOS : p-channel MOS
3. CMOS : complementary MOS
   = NMOS + PMOS

• 可同時製做出NMOS及PMOS的ICs製程技術





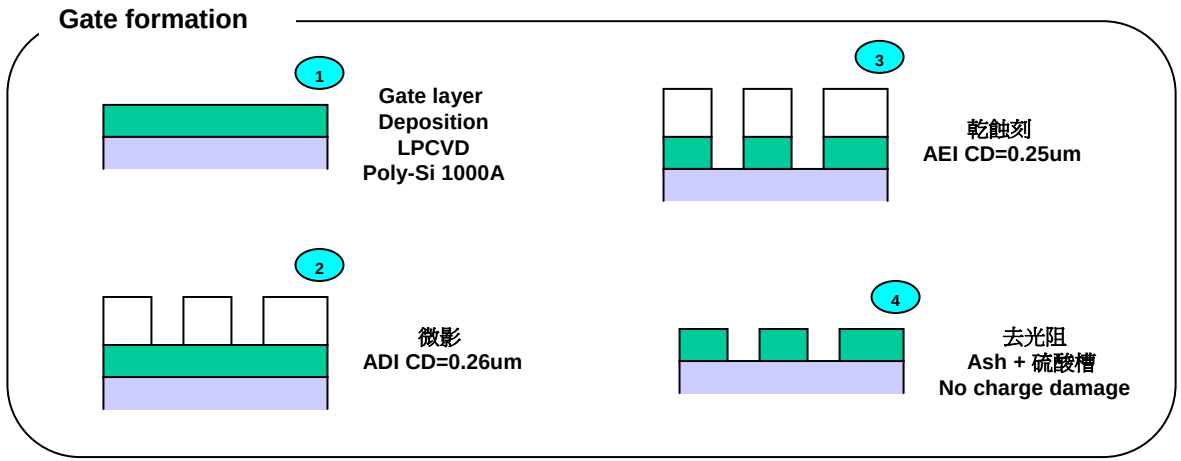
** channel : 位於gate下面, 是電流流通的通道,
由施加於gate上的電壓來控制形成與否

製程整合(process integration) :

[1] 定義 –

將必需且適當的製程步驟(process steps)依正確的順序(sequence)組合起來, 以獲得電路設計者(designer)所預期的電特性及功能(function)

- 必需的 → 避免多餘的步驟, 以降低成本, 減少cycle time及出錯機率
- 適當的 → 符合製程參數的, 最佳的方式的
- 正確順序的 → 如gate formation



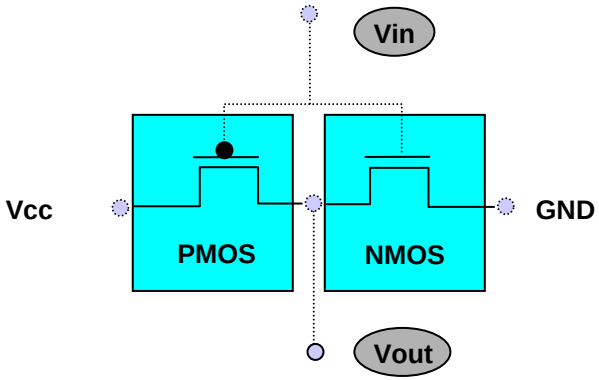
[2] 製程流程(process flow) –

分成 : 前段 (front-end) – MOS製做 → 完成MOS所有的必要條件

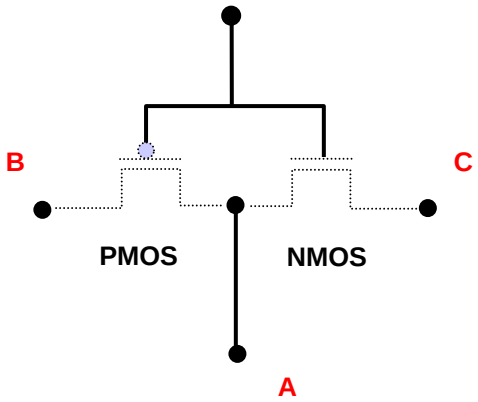
後段 (back-end) – 金屬連線製做 → MOS間的連線及ICs對外的連結開口

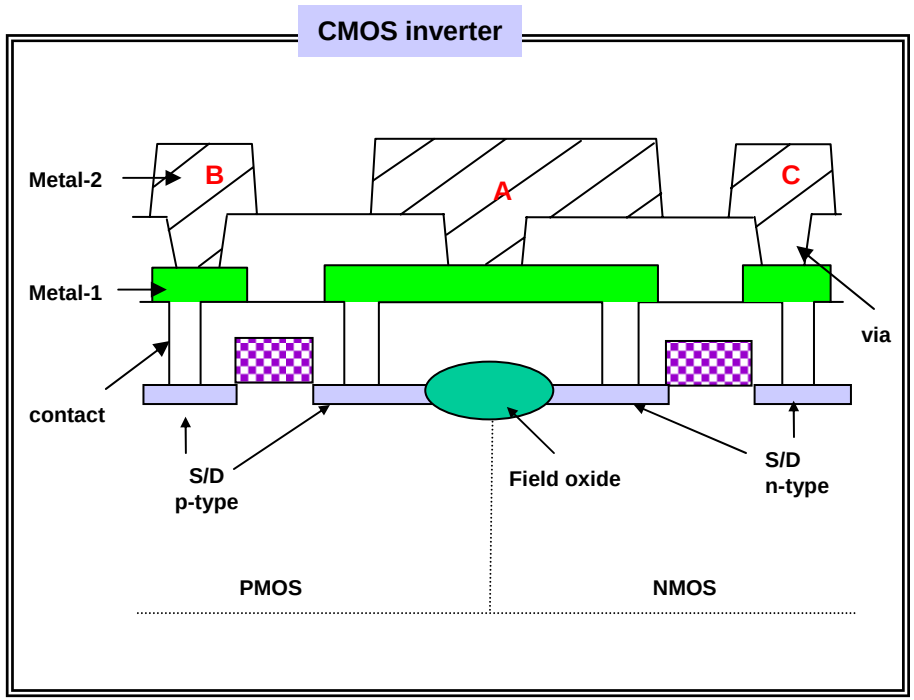
[3] CMOS製程流程 –

1. 前段 (front-end) – MOS製做
→ 完成MOS所有的必要條件



2. 後段 (back-end) – 金屬連線製做
→ MOS間的連線及ICs對外的連結開口

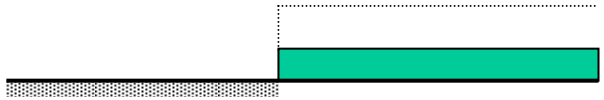




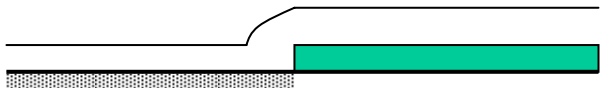
3. Process flow :

(1) pad-ox → thermal oxidation (300A), release Si3N4 stress
Si3N4 deposition → LPCVD (1750A), CMP strop layer,
N- well implant mask

(2) N-well Litho. → MUV, define N-well area
SiN RIE → dry etching, stop on pad-oxide
PR strip → SH (H2SO4 + H2O2)
N-well implant → P implant, N-well doping

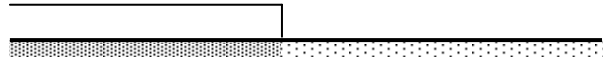


(3) TEOS deposition → PLCVD, P-well implant mask

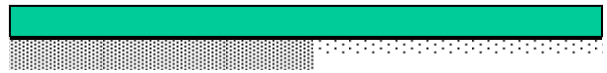


(4) CMP → oxide CMP, strip oxide over SiN

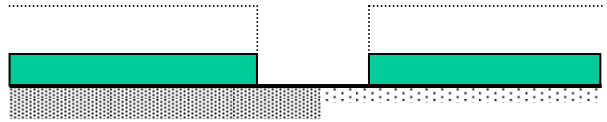
(5) SiN strip → wet etching(hot H_3PO_4) , open P-well area
N-well implant → B implant, N-well doping



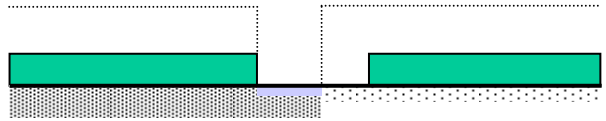
(6) Oxide strip → wet etching, all oxide remove
2nd pad-oxide → thermal oxidation(200A),
release SiN stress
SiN deposition → LPCVD, thermal oxidation mask



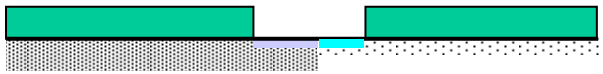
(7) AA Litho. → DUV, Active area definition
SIN etching → dry etching, stop on oxide
PR strip → SH



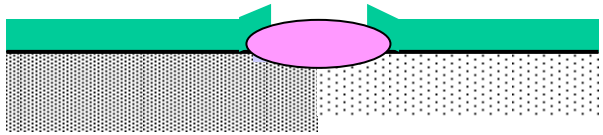
(8) N+ channel stop Litho. → MUV, open channel implant area
N+ channel stop implant →防止寄生電晶體形成
PR strip → SH



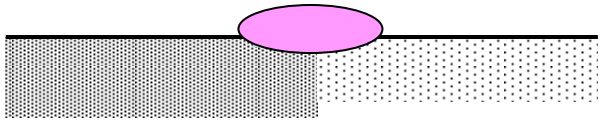
(9) P+ channel stop Litho. → MUV, open channel implant area
P+ channel stop implant →防止寄生電晶體形成
PR strip → SH



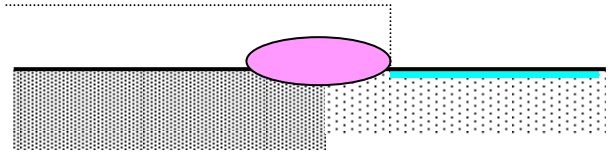
(10) Field oxidation → thermal oxidation(6500A),
filed oxide formation
drive well dopant in



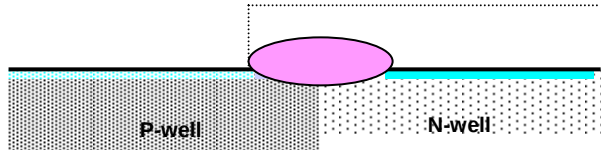
(11) SiN strip → wet etching
SAC oxidation → thermal oxidation, avoid Kooi effect
implant butter layer



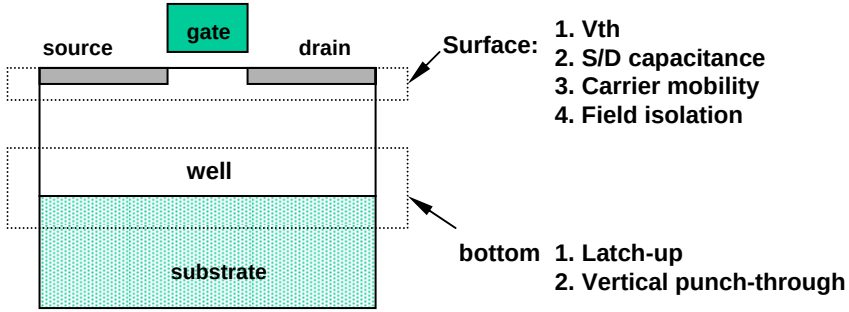
(12) VTN litho. → open NMOS area
VTN implant → 調整NMOS threshold voltage
PR strip → SH



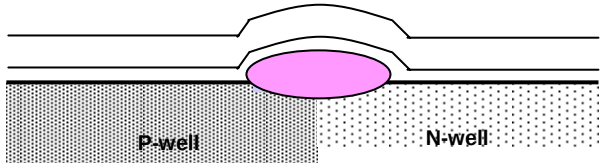
(13) VTP litho. → open PMOS area
VTP implant → 調整PMOS threshold voltage
PR strip → SH



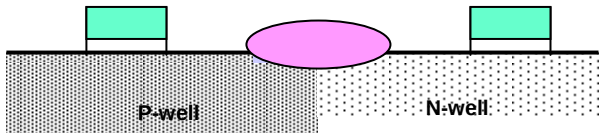
Well的濃度與MOS的電性有決定性的關係：



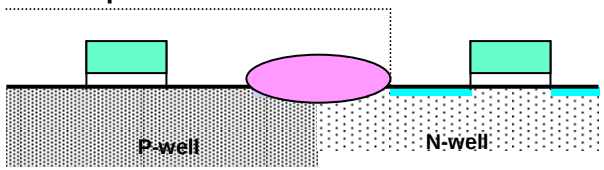
(14) Gate oxide formation → thermal oxidation(100A)
poly-Si deposition → LPCVD(2500A), gate material
WSi deposition → LPCVD, reduce gate Rs



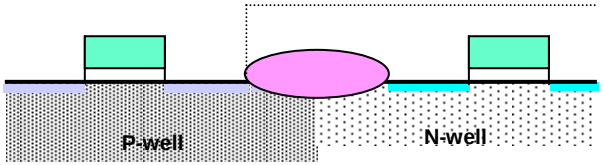
(15) Gate Litho. → DUV, define gate pattern
gate etching → dry etching, stop on oxide
PR strip → SH



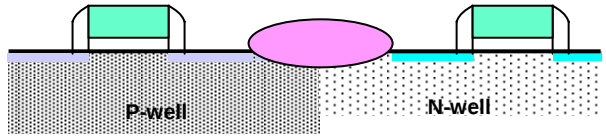
(16) N-LDD litho. → MUV, define NMOS area
N-LDD implant → P implant, reduce hot carrier
PR strip → SH



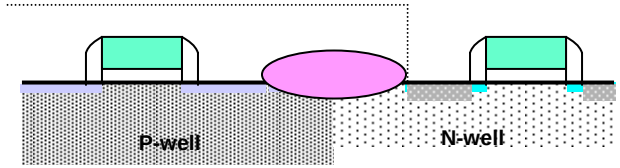
(17) P-LDD litho. → MUV, define PMOS area
P-LDD implant → B implant, reduce hot carrier
PR strip → SH



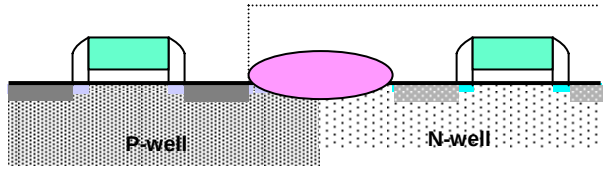
(18) Spacer deposition → LPCVD, spacer material
spacer etching → dry etch



(19) N+ S/D Litho. → MUV, open NMOS area
N+ implant → S/D doping, dopant is As
PR strip → SH

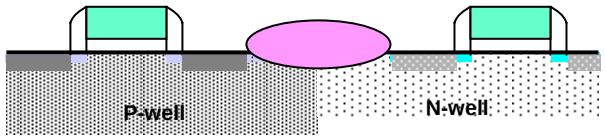


(20) P+ S/D Litho. → MUV, open PMOS area
P+ implant → S/D doping, dopant is BF^{+2}
PR strip → SH

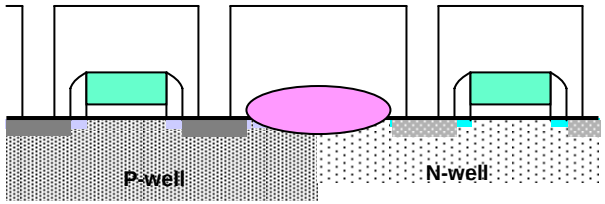


前段製程

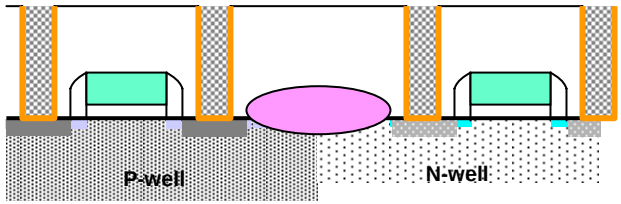
(20) BPSG deposition → APCVD, isolation, Na gettering
BPSG flow → gap fill
CMP → oxide CMP, 全面平坦化(for contact litho.)



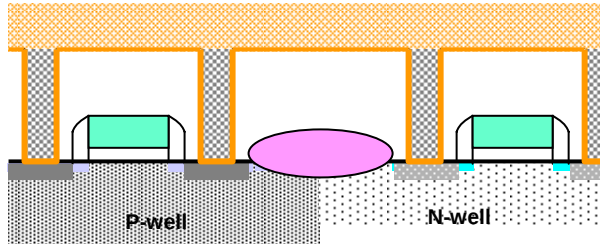
(21) Contact Litho. → DUV, define contact
contact etching → dry etch
PR strip → SH



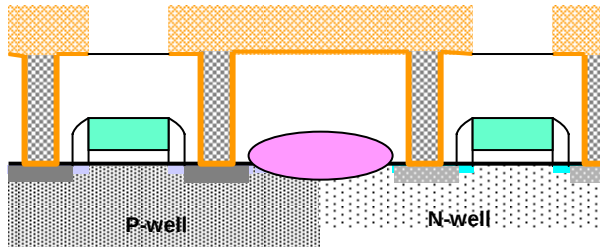
(22) Barrier metal deposition → sputtering, Ti/TiN
W deposition → LPCVD
CMP → W-CMP, plug formation



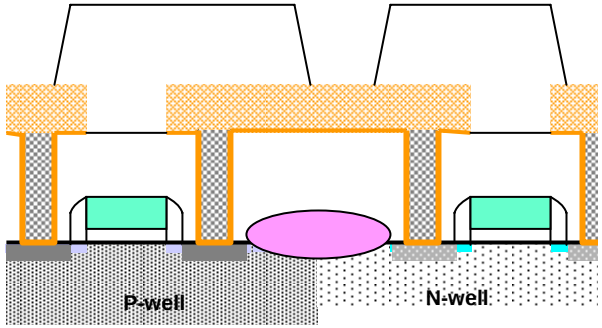
(23) BM deposition → sputtering, Ti/TiN
metal deposition → sputtering, Al-Cu, metal-1



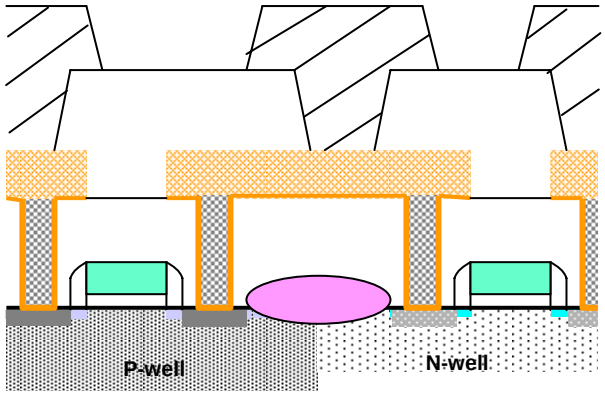
(24) M1 Litho. → DUV, define M1 pattern
M1 etching → dry etch
PR strip → Ash



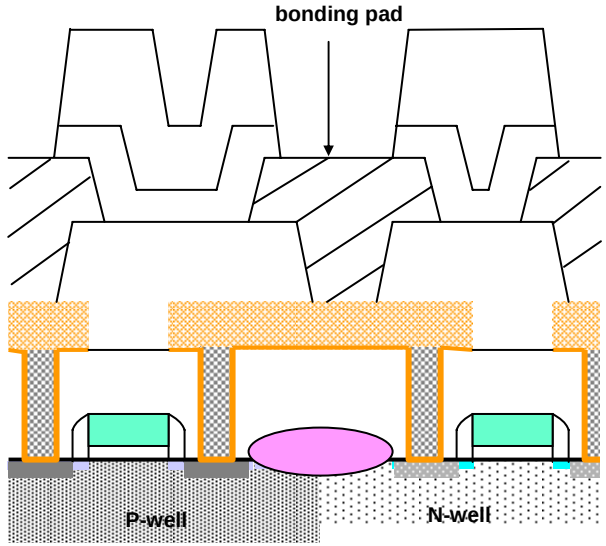
(25) TEOS deposition → PECVD, isolation
CMP → oxide CMP
Via Litho. → define via
Via etching → dry etching, open via
PR strip → Ash



(25) BM deposition → sputtering, Ti/TiN
Metal deposition → sputtering, Al-Cu, M-2
M2 Litho. → define M2 pattern
PR strip → Ash



(26) TEOS deposition → PECVD, release SiN stress
SiN deposition → PECVD, protection layer
bonding pad Litho. → define bonding pad area
etching → dry etching
PR strip → Ash



製程規格與 Design rule

製程規格(process specification) :

[1] 爲何需要SPEC. –

精確定義每道製程步驟所要達到的目標, 如

Thermal oxidation
- 厚度 (thickness)
- 屈折律率(refractive index)
- 蝕刻率(etching rate)
- 氧化層中電荷(charge)
- oxide/Si 界面(interface)
- 氧化層介電破壞(breakdown)
- 製程溫度(processing temp.)
- …

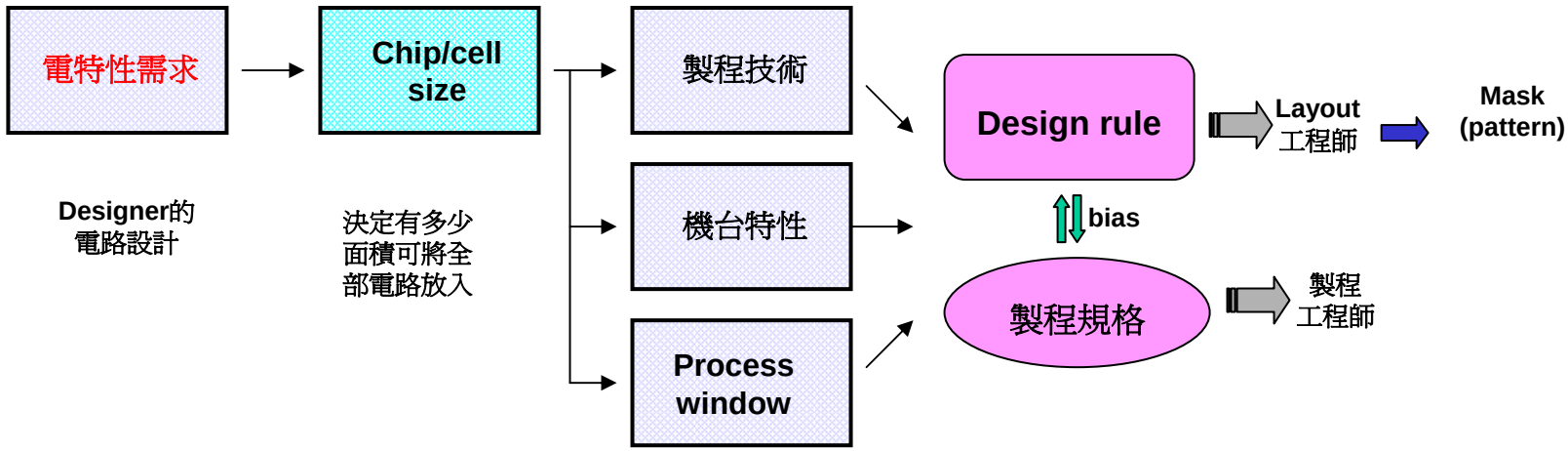
Thin film
- 厚度
- 均勻度
- 蝕刻率
- 填洞 (gap fill)能力
- 介電常數(dielectric constant)
- 製程溫度
- 應力(stress) …

Litho.
- ADI CD
- alignment
- 均勻度
- PR厚度
- PR profile
- soft/hard bake temp.
- …

Etching
- AEI CD
- 選擇比
- 均勻度
- profile
- Charge damage
- process temp.
- etching rate
- …

CMP
- 研磨率
- 選擇比
- 均勻度
- dishing
- particle
- …

[2] 如何訂出SPEC. ? –

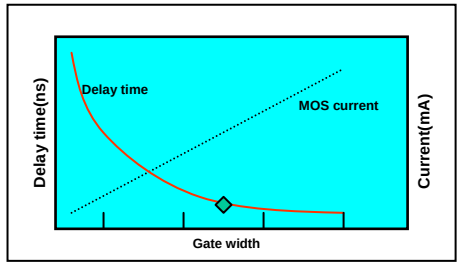


製程規格與 Design rule

[3] 實例 – 0.25um SDRAM gate Rs(sheet resistance)

Designer的電路設計 → Delay time = 8ns
Gate Rs = 30 +/- 10 ohm/sq

Chip/cell size → Chip size = 6.3*12.6 mm^2
Cell size = 0.55*1.1um^2



0.225~0.275um gate width

製程技術 → Poly-Si gate : Rs 100 ohm/sq
Polyside gate(poly+Wsi) : Rs <30 ohm/sq, →
- poly-Si厚度: 1000+/-100A
- Wsi厚度 : 550+/-55A

機台特性 → Dry etching bias : 0.01um
對光阻選擇比 = 1 : 4 →
- ADI CD = 0.24+/- 0.025um
- AEI CD = 0.25+/- 0.025um
- PR厚度 = 0.75um

Process Window check → Litho. → • DOF window check

BPSG gap fill能力 → • x-SEM check → gate spacing >=0.2um